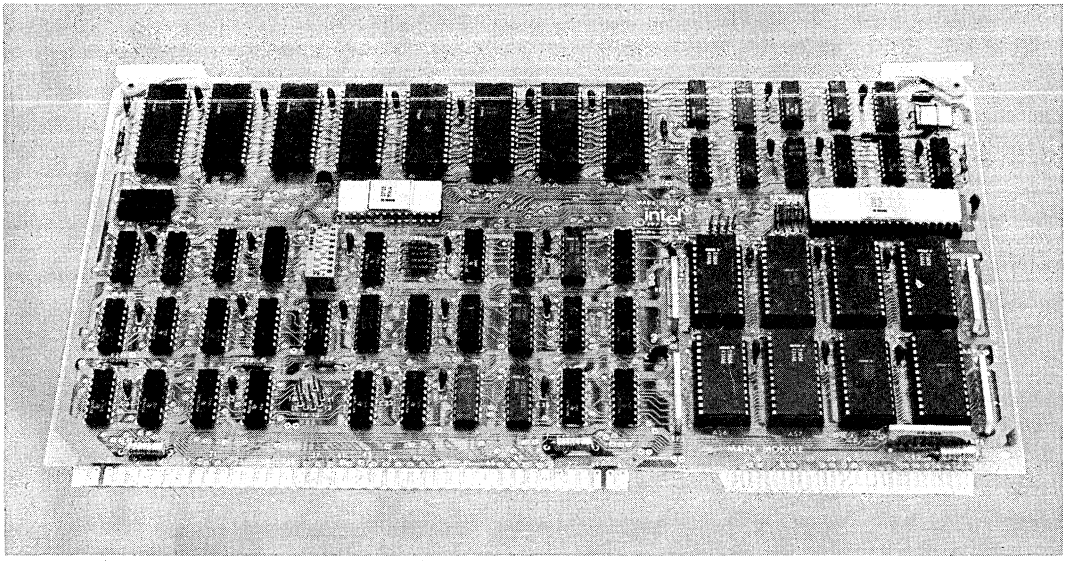
iSBC 310A
HIGH SPEED MATHEMATICS UNIT

- **Provides iSBC 80 high speed mathematical functions**
- **Performs functions independently and concurrently with iSBC 80 Single Board Computer functions**
- **Fixed point integer arithmetic**
  - **— 16- and 32-bit format**
  - **— Multiply and divide**
  - **— Extended divide**
- **Floating point arithmetic**
  - **— Intel standard 32-bit format**
  - **— Add, subtract, multiply, divide**
  - **— Square and square root**
- **Compare and test operation**
  - **— Relative to zero**
  - **— Relative to floating point constant**
- **Float-to-fix and fix-to-float conversions**
- **Multimaster access — multiple masters may access iSBC 310A via system bus**
- **Single +5V power requirement**

The iSBC 310A High Speed Mathematics Unit is a member of Intel's complete family of OEM computers and expansion modules. The iSBC 310A acts as an intelligent slave processor to one or more iSBC computer masters as it performs its high speed arithmetic functions. It plugs into a standard iSBC 604/614 cardcage to interface directly into any iSBC 80 single board computer. Designed to increase the computational throughput of all computers in the iSBC 80 family, the iSBC 310A utilizes Intel's high speed Series 3000 Bipolar Microprocessor. The iSBC 310A performs arithmetic functions an order of magnitude faster than is possible with software routines. Standard operations include floating point add, subtract, multiply, divide, square, and square root; fixed point integer multiply, divide, and extended divide; and conversions between fixed and floating point representations, as well as test, compare, and argument exchange.



FUNCTIONAL DESCRIPTION

iSBC 80 single board computers communicate with the iSBC 310A using I/O and memory read/write commands. To pass arguments from the iSBC 80 to the iSBC 310A, a memory write command is used for each byte to be loaded into the iSBC 310A's working registers. An operation command is then given to the iSBC 310A by using an output instruction to pass the appropriate opcode. The mathematics unit will then perform the function independently from the single board computer; therefore, any iSBC 80 can continue to operate while the iSBC 310A is performing its arithmetic operations. Upon completion of its designated operation, the high speed mathematics unit notifies the iSBC 80 via an interrupt or by setting a status bit. The resultant data can then be read by the iSBC 80 via a memory read command to the proper memory address.

Arithmetic Functions

The iSBC 310A provides a full complement of arithmetic functions which operate on 16- and 32-bit unsigned fixed point integers, 32-bit signed fixed point integers, and 32-bit single precision floating point numbers. These functions are detailed in Table 1. The results of comparison operations are described in the operation results section.

Status Byte

The iSBC 310A may be operated in either an interrupt driven or polled mode. Three status indications are available:

Busy — The iSBC 310A is currently processing an arithmetic command, and cannot respond to further requests.

Complete — The iSBC 310A has completed an operation without an error. This line may be connected to an interrupt level via an on-board jumper.

Error — The iSBC 310A has completed an operation which results in an error condition. This line may be connected to an interrupt level via an on-board jumper.

Result Byte

After completion of an operation, a result byte may be read. This byte indicates the error conditions where applicable (see Specifications), and the results of a compare or test operation.

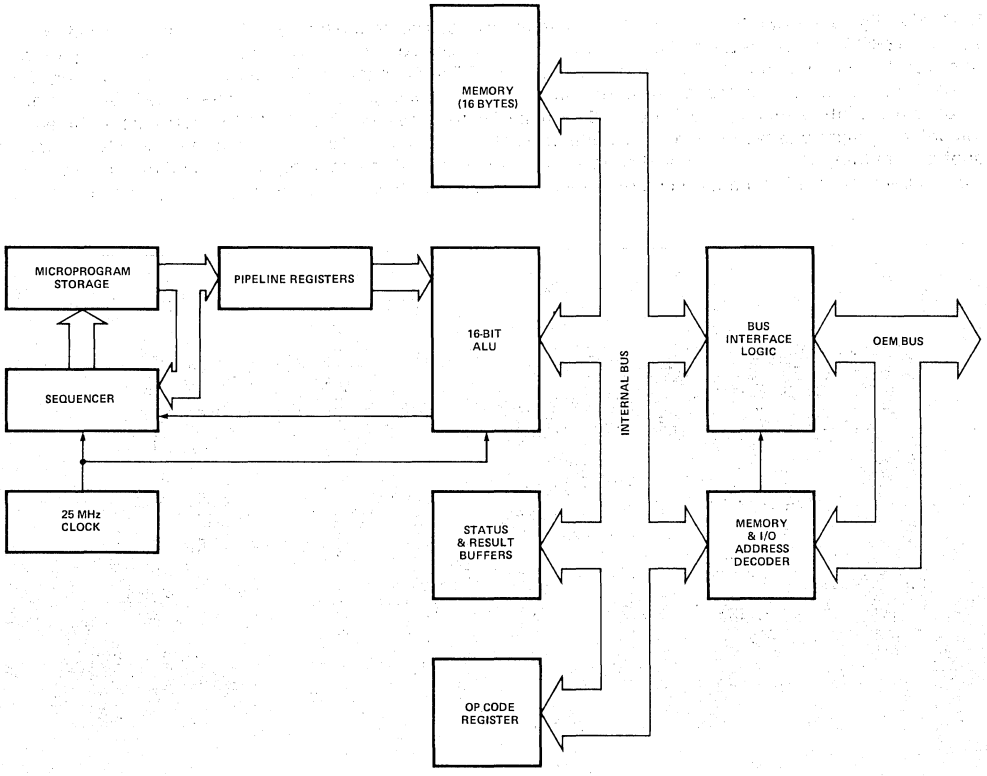


Figure 1. iSBC 310A Block Diagram Showing Functional Components

Table 1. ISBC 310A Arithmetic Functions

Operation	Op Code	Max Time[1] (μs)	Notes[2]
Fixed point multiply (MUL)	0	19	$M_1 = m_1 * m_1$
Fixed point divide (DIV)	1	28	$m_1 = m_1/M_2$, m_2 = remainder
Extended fixed point divide (EDIV)	E	94	$M_1 = M_1/m_2$, M_2 = remainder
Floating point multiply (FMUL)	2	91	$X_1 = X_1 * X_2$
Floating point divide (FDIV)	3	102	$X_1 = X_1/X_2$
Floating point add (FADD)	4	56	$X_1 = X_1 + X_2$
Floating point subtract (FSUB)	5	56	$X_1 = X_1 - X_2$
Square (FSQR)	6	91	$X_1 = X_1^2$
Square root (FSQRT)	7	199	$X_1 = \sqrt{X_1}$
Fixed-to-float-conversion (FLOAT)	8	89	$X_1 = N_1$
Float-to-fixed-conversion (FIX)	9	81	$N_1 = X_1$
Compare (FCOMP)	A	5	Compare X_1 and X_2
Test (FTST)	B	5	Compare X_1 and 0.0
Exchange (EXCH)	F	4	Exchange arguments (fixed or floating)

Notes
1. Does not include register setup time
2. m — 16-bit unsigned fixed point integers; M — 32-bit unsigned fixed point integer; N — 32-bit two's complement signed fixed integer; X — 32-bit single precision floating point number

SPECIFICATIONS

Arithmetic Functions

See Table 1

Formats

Single Precision Floating Point (32 Bits)

Memory Location		
Base Address (M)	$F_7 - F_0$	
M+1	$F_{15} - F_8$	
M+2	E_0	$F_{22} - F_{16}$
M+3	S	$E_7 - E_1$

where: S = sign bit
0 = positive
1 = negative
$E_2 - E_0$ = biased exponent (8 bits) (bias = $7F_H$)
$F_{22} - F_0$ = fraction (23 bits)

Note
F is always normalized (i.e., a "1" is assumed in the highest bit position), yielding an effective 24-bit fraction.

Fixed Point Integer (16-Bit)

Memory Location	
Base Address (M)	$F_7 - F_0$
M+1	$F_{15} - F_8$

where:
$F_{15} - F_0$ = 16-bit integer

Extended Precision Integer

Memory Location		
Base Address (M)	$F_7 - F_0$	
M+1	$F_{15} - F_8$	
M+2	$F_{23} - F_{16}$	
M+3	S	$F_{30} - F_{24}$

where: S = sign bit
$F_{30} - F_0$ = two's complement integer

Result Byte

Contains the following information:

7	6	5	4	3	2	1	0
=	>	<	R	R		ERR	

where: R is reserved for future use
= is equal (for FCOMP and FTST)
> is greater than (for FCOMP and FTST)
< is less than (for FCOMP and FTST)

and: ERR is a 3-bit error code that specifies one of the following error conditions:

000 No error
001 Divide by zero
010 Square root of negative number
011 Overflow
100 Underflow
101 First argument valid
110 Second argument valid
111 Reserved

Status Byte

Contains the following information:

7	6	5	4	3	2	1	0
R	R	R	R	R	E	C	B

where: R is reserved for future use
B is busy
C is operation complete without error
E is operation complete with error

Addressing

I/O Addressing — Used to pass operation codes, memory address boundaries, and result and status bytes between host processor and iSBC 310A.

Port Address	Output	Input
Base (P)	OP CODE	R
P+1	MEM LOW	Result byte
P+2	MEM HIGH	R
P+3	R	R
P+4	R	R
P+5	R	R
P+6	R	R
P+7	R	Status byte

where: P = I/O base address of X0 or X8 (where X = any hex digit)
R = reserved for iSBC 310A usage
OP CODE = mathematic commands (see Table 1)
MEM LOW, MEM HIGH = programmable base address (see Memory Addressing)

Memory Addressing — Sixteen memory locations are used; the first eight are used for argument/result storage; the second eight are reserved for future use. Memory addresses are assigned from the host processor via an I/O output instruction (see I/O Addressing). MEM LOW (the lower address byte) must be X0 (where X is any hex digit). MEM HIGH (the upper address byte) may be any value.

Interrupts

Interrupts are generated on operation complete and operation error. Either one or both interrupts may be connected to any of the 8 interrupt levels on the iSBC 80 bus via jumper selection.

Bus Interface

All signals are TTL compatible.

Bus Connector

Bus Connector — 86-pin, double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Viking 3KH43/9AMK12

Physical Characteristics

Width — 12.00 in (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (340.5 gm)

Electrical Characteristics

DC Power Requirements

V_{CC}	I_{CC}
5V ± 5%	6.7A max; 4.9A typ

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Equipment Supplied

High speed mathematics units
Standard preprogrammed ROMs (installed)
Schematics
Assembly drawing

Reference Manual

9800410A — iSBC 310A Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 310A	High Speed Mathematics Unit